High Throughput Low Stress Air Jetting Carrier Release for RDL-First Fan-Out Wafer-Level-Packaging

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***Abstract*—Fan-out wafer level packaging (FOWLP) not only provides simplified supply chain management and lower cost structure, but also enables thinner profile and heterogeneous system integration. FOWLP is becoming increasingly significant and is projected to drive growth in advanced packaging for the foreseeable future.**

There are many different processing technologies for fabricating FOWLP. One common key practice, which is very different from fan-in wafer level packaging, is the use of a temporary carrier to support wafer-level fabrication. The redistribution-layer (RDL) first approach is one of two mainstream processing technologies for FOWLP at present. One benefit is that the RDL is fabricated with direct support of a flat, rigid carrier prior to the occurrence of molding warpage and die shift. However, the RDL-first approach requires a carrier sacrificial layer that can withstand high-temperature/high-vacuum RDL build-up fabrication. Determined by adhesive chemistry's availability, the present forms of RDL-first FOWLP processing require carrier release by laser ablation, thus further limiting the choice of carrier to glass. At present, laser debonding for RDL-first FOWLP is a very costly and lengthy process.

This paper presents a design for optimizing and processing a carrier-sacrificial layer that is compatible not only with current RDL-first FOWLP fabrication, but also enables the carrier's instant release by air jetting at room temperature. This air-assisted mechanical release of the carrier minimizes debonding stress on the wafer surface without localized heating and burning, and provides even more stress relief for larger carriers.

A fan-out WLP process flow with air jetting carrier release is presented and evaluated. Key material properties of the current sacrificial-layer design are also analyzed. *(Abstract)*

Keywords-FOWLP; RDL-First; Debonding; Temporary Support; Air Jetting; Low Stress; Low Warpage (key words)

I. INTRODUCTION

As the demand for thinner, faster, more powerful but better heat dissipation continues to drive the integrated circuits (IC) packaging market, fan-out wafer level packaging (FOWLP) emerges as an attracting packaging technology for its high degree of heterogeneous integration and wide range of applications, e.g., FPGA, GPU, application processors for mobile devices, RF/Wi-Fi modules, power amplifier (PA) modules, etc. FOWLP delivers smaller package footprints and increased number of interconnects with improved electrical and thermal performance.

As Taiwan Semiconductor Manufacturing Co. (TSMC) successfully implemented its integrated fan-out (InFO) packaging technology for Apple's A10 application processor in the new iPhone7, many new players with a variety of FOWLP designs are entering the semiconductor packaging

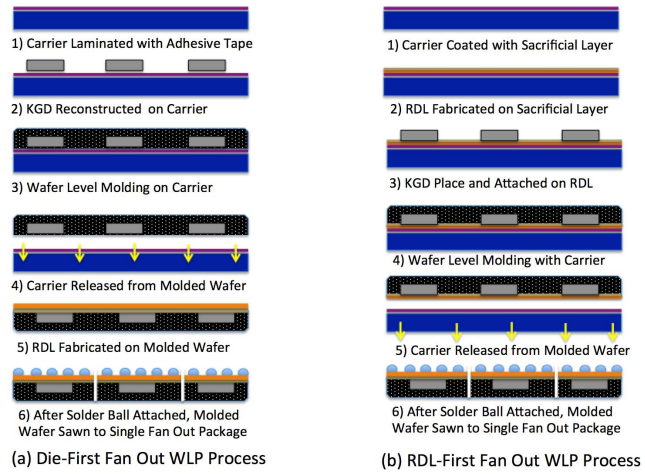


Figure 1. (a) Die-first FOWLP process flow, (b) RDL-first FOWLP process flow.

market. The adaptation of Apple's A10 on FOWLP represents a paradigm shift for the fan-out industry. It is confirmed that the adaption of InFO packaging has led to improvement of more than 15% in signal speed, 9% in thermal performance, and 18% reduction in package thickness, and has also enabled a much faster main memory interface to the logic die [1]. This performance improvement is roughly equivalent to that expected between successive foundry node reduction (e.g., the change from 14 nm to 10 nm), but is driven by a new packaging technology rather than a new process.

The FOWLP process was first developed 10 years ago. Infineon first introduced an embedded wafer-level ball grid array (eWLB), first commercialized in an LG cellphone in 2009. While there are various processing flows for constructing different configurations of FOWLP package, two major categories best describe the FOWLP process technology, namely die-first (molding first) process and die-last (RDL-first) process (see Fig. 1) [2][3][4]. The die-first process starts with a carrier laminated with double-sided tape to which individual known good die (KGD) is attached. Wafer-level molding encapsulates and embeds the die on one side of the tape. The carrier and tape are subsequently removed, leaving the die embedded in the mold. Then, the so-called reconstituted wafer is flipped upside-down. The die is exposed at the top, onto which RDL is fabricated. Solder balls are attached after the RDL process, and then the reconstituted molded wafer is singulated to individual fan-out packages. The RDL-first (die-last) process begins with sacrificial layer coating on the carrier. The RDL layers are fabricated on the sacrificial layer, followed by attaching KGD to the RDL. Wafer-level molding is then conducted to encapsulate the reconstituted die. The carrier and sacrificial layer are then subsequently removed, leaving the RDL of the reconstituted mold wafer exposed. After solder balls are attached, the reconstituted mold wafer is then singulated to individual fan-out packages.

In the die-first process, the RDL is produced after removing the carrier, thus the yield loss in RDL fabrication occurs after the KGD are attached, subjecting KGD to additional loss. Also, die-shift during molding and warpage occurring after curing the molding compound represent insurmountable obstacles for producing a RDL with line/width resolution smaller than 10 µm. On the other hand, in the RDL-first process, the RDL is created and tested first while supported by the carrier, thus enabling a much higher RDL line/width resolution. Furthermore, the RDL can be tested before KGD are mounted, thus avoiding the loss of good tested die due to the RDL process. It is commonly agreed that the RDL-first process is preferred for high-value, larger I/O count with higher-resolution fan-out packaging.

II. TEMPORARY SUPPORT SYSTEM FOR RDL-FIRST PROCESS

In the traditional chip-first fan-out approach, the temporary wafer support system consists of a carrier and double-sided adhesive tape to hold the chip tightly during molding. The molding temperature must be low in order to ensure thermal stability of the tape; however, lower molding temperature greatly reduces package's long-term reliability.

In the RDL-first fan-out approach, the temporary support system provides a platform upon which to construct the fan-out package. An RDL passivation layer needs to be fabricated directly onto the surface of the temporary support. This requires much higher thermal stability than can be provided by the double-sided tape in the die-first process. Currently, a temporary support system for the RDL-first approach consists of a rigid carrier and a sacrificial layer that is coated onto the carrier surface to facilitate the carrier's removal at a later stage. After the sacrificial layer is coated, a typical RDL-first process includes permanent dielectric polymer coating & baking, photolithography, sputtering, electroplating, etching, chip attachment and wafer-level compression molding, etc. The sacrificial layer must withstand all the above processes in combination with temperature cycles & harsh chemical batch processes. In the final stage, the carrier and sacrificial layer need to be removed without damaging the RDL structure prior to solder ball attachment. Given these requirements, there are very limited choices for temporary support systems in the RDL-first fan-out process.

A. Laser Release

Currently, the most common debonding mechanism employed for RDL-first FOWLP is laser-assisted ablation release. This debonds the carrier by employing ablation to break the bonds of the polymer chain (see Fig. 2), thus requiring the sacrificial layer to be highly absorptive within the wavelength of the laser beam. Also, laser release requires the carrier to be highly transparent, such that glass is the only practicable choice of carrier material. The ablation process is conducted through line scan, and introduces localized heating to the wafer surface, which would be of concern due to local thermal stresses. Furthermore, the laser release method is very costly, and is thus limited to high-density, high-I/O, high-end applications.

B. Air Jetting Release for RDL-First Process

The concept of air jetting to debond a wafer stack was first introduced in 2016 [5]. Unlike mechanical peeling, which generates significant peeling stress on the wafer

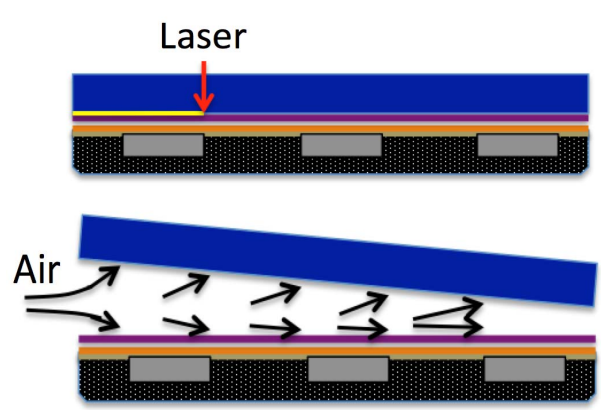


Figure 2. Laser and air debonding mechanisms.

surface, air-jet debonding introduces air streams between the carrier and wafer surface, thus pushing carrier up-lift from underneath and compressing the wafer surface downward (see Fig. 2). In air debonding, silicon or other carrier materials can all be used for better matching the coefficient of thermal expansion (CTE), thus greatly reducing warpage of the bond stack in process. Furthermore, the airflow results in the most uniform stress distribution across the wafer, and the debonding is instant and conducted at room temperature.

III. THE SACRIFICIAL LAYER FOR AIR JETTING RELEASE

The key to successful carrier release with air jetting is the sacrifice layer material and its controlled thermal and mechanical properties. The FOWLP is built upon the sacrificial layer with support of a carrier. In general, the sacrificial layer material has to satisfy the following basic requirements: (1) thermally stable at all processing temperatures, (2) resistant to all processing chemicals, (3) sufficient mechanical strength and void-free in all FOWLP processing steps, (4) able to form uniform and tack-free layer on carrier, and (5) can be completely removed after carrier release. Z-Coat 211 is a polyimide (PI) based polymer coating developed as the sacrificial layer for FOWLP.

A. Thermostability and Tack-Free at High Temperature

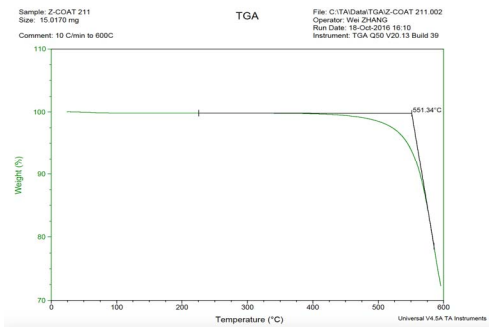
Thermostability often refers to the ability to resist decomposition and outgassing during thermal processing. A common method for characterizing a material's thermostability is thermo-gravimetric analysis (TGA), which measures weight loss as a function of temperature increase, or as a function of time at a fixed temperature. Z-Coat 211 is a thermosetting polymer that remains tack-free after curing, even at high temperature. Fig. 3 shows the weight loss of Z-Coat 211 (a) at a constant heating rate of 10 °C/min up to 600°C, and (b) at fixed temperature of 300 °C over a period of 120 minutes. The results show that Z-Coat 211 is highly stable up to 425 °C, with a decomposition temperature around 550 °C. Its weight loss is less than 0.3% after a two-hour bake at 300°C.

Fig. 3 (c) shows a high-temperature PI tape peeling from Z-Coat 211 surface at 250 °C. It appears that the peeling interface is between silicone adhesive of the PI tape and Z-Coat 211 without any residue or cohesive failure. The Z-Coat 211 maintains its integrity very well at 250 °C.

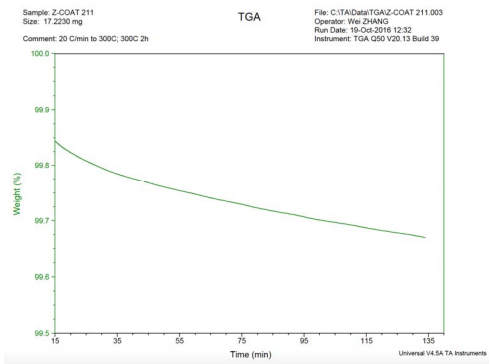
B. Chemical Resistance

As the FOWLP fabrication process involves many steps of chemical etching, smoothing, stripping, and cleaning, the sacrificial layer is required to maintain the highest integrity against all processing chemicals involved.

The chemical resistivity of Z-Coat 211 has been tested extensively after curing on carrier's surface. Table I summarizes test results under various testing conditions, showing that Z-Coat 211 appears to have excellent chemical resistance for FOWLP applications.



(a) Rate = 10 °C /min



(b) Temperature = 300 °C

(c) PI tape peeling from Z-Coat 211 surface at 250°C

Figure 3. TGA plot of Z-Coat 211 (a) at constant heating rate 10 °C/ minute and (b) at constant temperature 300 °C and (c) Tape peeling from Z-Coat 211 surface at 250 °C.

TABLE I. Z-COAT 211 CHEMICAL RESISTANCE

Chemicals	Test Condition	Result
PGMEA	25 °C soak 30 minutes	Weight Loss < 1%, Surface no Change
0.045% KOH	25 °C soak 30 minutes	
Al Hydroxide	40 °C soak 60 minutes	
10% Oxalic Solution	50 °C soak 60 minutes	
2.38% TMAH	25 °C soak 30 minutes	
Hydrofluoric 6N	25 °C soak 30 minutes	
Acetic Acid 6N	25 °C soak 30 minutes	
Acetone	25 °C soak 30 minutes	
NMP	50 °C soak 30 minutes	
DMAC	25 °C soak 30 minutes	
Isopropanol	25 °C soak 30 minutes	
H2O:NH4OH:H2O2	25 °C soak 30 minutes	
(5:1:1)		
H2O:H2SO4:H2O2	25 °C soak 30 minutes	
08:01:01		
H2O2 30%	25 °C soak 30 minutes	

C. *Adhesion to Carrier*

Z-Coat 211 is designed as the sacrificial layer to connect the carrier during FOWLP fabrication. Its peel adhesion and shear strength to the carrier are addressed below:

1) *Peel Adhesion to Silicon Carrier*

Z-Coat 211's peeling adhesion on a mirror silicon carrier was tested using a Mark-10 peel tester with a force gauge capable of 0.05 g resolution. The average of ten test trials is shown in the second column from right of Fig. 4, with a comparison with other known tapes. The peel adhesion is about 7~8 gF/inch, approximately 20% of the non-UV blue dicing tape used in the test and similar to low-adhesion UV dicing tape (after UV).

2) *Shear Strength to Silicon Carrier*

In our shear strength study, Z-Coat 211 was coated and cured on a bare silicon dummy wafer. The wafer was then cut into 5×5 mm pieces of die. Two dice were glued together on the Z-Coat 211 surface by high-strength double-sided tape, and then tested for die shear strength (Nordson Dage 4000 Bond tester). Fig. 5 shows the shear testing results of ten test samples. The results consistently showed that failure mode was as the delamination of carrier from the film, and the average shear force for the 5 mm stack is 2.58 kgF, equivalent to shear strength of approximately 1000 kPa.

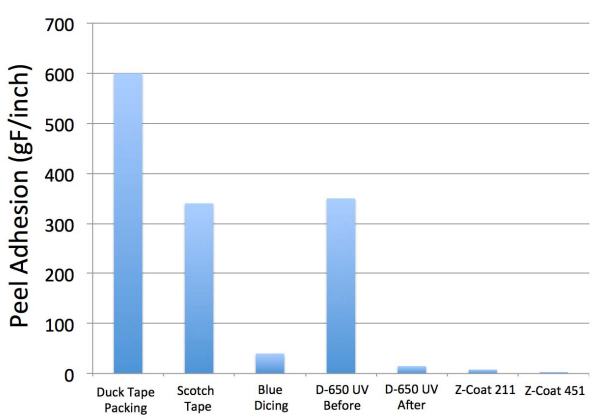


Figure 4. Peel adhesion of Z-Coat 211 compared to other known tapes.

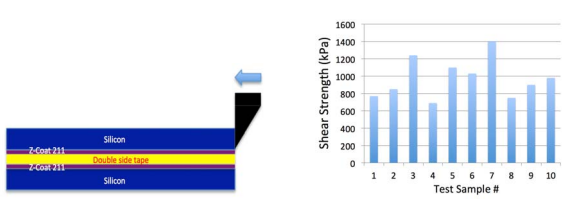


Figure 5. Shear strength of Z-Coat 211 on silicon carrier.

IV. PROCESS EVALUATION

The process evaluation in this chapter represents a collaboration between MMI and the Industrial Technology of Research Institute (ITRI) in Hsinchu, Taiwan. The first trial run focused on key aspects of the FOWLP process, including sacrificial layer coating, passivation layer coating, thin metal film deposition, wafer-level film molding, carrier release with air jetting, and sacrificial layer cleaning. Fig. 6 summarizes processing-step in this trial evaluation. Step 1), 2), 9) and 10) were conducted in MMI, and other steps were done in ITRI. 200 mm mirror dummy silicon wafer was used as carrier.

A. *Sacrificial Layer Spin-Coating*

Z-Coat 211 is supplied as a solvent-based spin-on liquid solution. After coating, it is baked at a stepped temperature profile to form a smooth, uniform, void-free dry film layer. The recommended baking schedule for Z-Coat 211 is at 75 °C and 150 °C for 1 minute each, then 200 °C for 5 minutes to completely remove the solvent and cure. Z-Coat 211 is a thermosetting polymer with onset curing temperature around 120 °C. After curing, it appears as yellowish film (Fig. 7) and stays dry at temperature below its T_g.

Fig. 8 (a) shows the thickness of the dry film after baking, as a function of spin speed. The thickness decreases with increased spin speed, and average dry film thickness is about 10 µm at 3000-rpm spin speed for 20 seconds. Fig. 8 (b) plots film thickness as a function of radial distance from the wafer center-point. The film coating appears to be very uniform, with TTV less than 1 µm across the whole wafer, which is well within the measurement error.

B. *Processing of RDL Passivation Layer*

The first layer material fabricated onto the sacrificial layer surface must be for RDL passivation, which is made of photo-imageable permanent dielectric material. There are

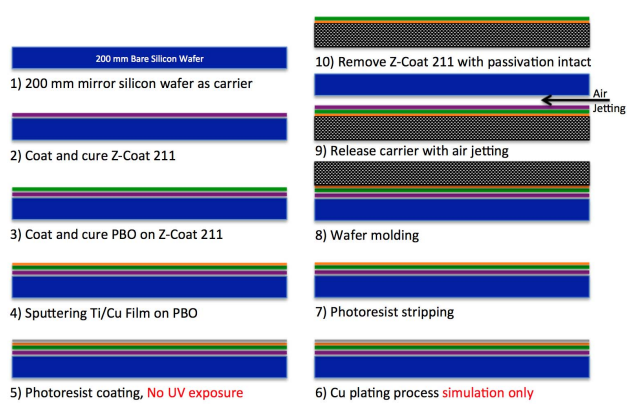


Figure 6. Process evaluated in this trial.

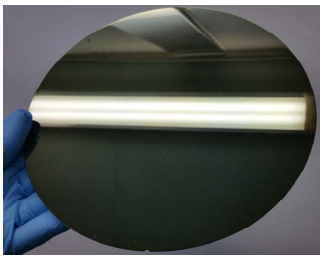
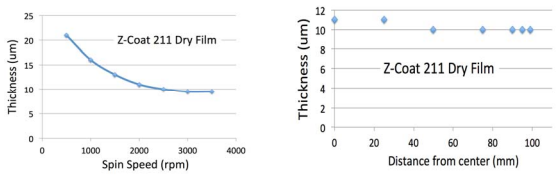


Figure 7. Z-Coat 211 cured on carrier.



(a) spin curve (b) thickness distribution

Figure 8. Z-Coat 211 thickness study.

many types of permanent dielectric polymers for RDL application, such as polyimide (PI), benzocyclobutene (BCB), polybenzoxazole (PBO) and epoxies. For each particular application, the appropriate material is selected according to processing capability, dielectric property, and mechanical reliability performance. At present, PI and PBO emerge as the major dielectric polymer types for FOWLP RDL applications.

Typical passivation layer processing includes spin-coating; soft bake; exposure UV light; development through spray, puddle or stream; hard bake cure at high temperature up to 300°C. The sacrificial layer must be able to withstand the above processes.

PBO process is evaluated on the current sacrifice layer design. The solvent system used in PBO is butyrolactone (BLO) and development utilized 2.38% TMAH puddle, followed by H_2O stream rinse. Pre-bake was 4 minutes at 110 °C and hard bake was 60 minute at 200 °C. No delamination or voiding was observed after the process. The thickness of the passivation layer is about 5 µm fully covering the sacrifice layer, and appears smooth.

C. *Sputtering Ti/Cu Metal Layer*

Sputtering is a physical vapor deposition (PVD) process to create a thin metal film, which is a common practice to deposit a seed/RDL metal layer in FOWLP. Among many processing parameters, high gas pressure and ultra-high-vacuum environment with elevated carrier temperature are major factors for controlling the quality of the thin film deposited.

Depending on the number of layers designed in the FOWLP process, there could be as many as six sputtering procedures procedure involved prior to carrier release. The current sacrificial layer design is required to withstand the sputtering process without exhibiting voiding or delamination between layers. Two separate sputtering tests were conducted: 1) sputtering Ti/Cu film on the passivation layer with the sacrifice layer Z-Coat 211 beneath; and 2) sputtering Ti/Cu film directly onto the Z-Coat 211 sacrificial layer. In both tests, 100 nm Ti with 300 nm Cu thin film were deposited on polymer coating with carrier temperature at approximately 120 °C and vacuum level of 0.0001Pa. No surface cracking, delamination or voiding was observed in either of the test scenarios.

D. *Wafer Level Molding*

Wafer-level compression molding was first developed specifically for FOWLP. Compared with traditional transfer molding, compression molding generates much lower force on reconstituted chips by immersing them in molten epoxy resin. The molding process is complete after the resin solidifies.

In traditional die-first FOWLP process, the RDL is created after wafer molding. As the molding material has different thermal-mechanical properties, the reconstituted wafer embedded with silicon chips exhibits significant non-planarity after cooling. Furthermore, the reconstituted chips shift under the shear force exerted by the flow of molten resin during the molding process. Warpage combined with die-shift represent insurmountable challenges to accurate alignment in RDL fabrication. In general, the die-first FOWLP approach is limited to above 10 µm line and width spacing resolution, and thus is not suitable for high-density FOWLP applications.

In RDL-first FOWLP process, the RDL is created with a support carrier and before wafer molding, thus eliminating the problems of die shift and warpage. It is commonly agreed that the RDL-first FOWLP approach is better suited to high I/O count, high-density, more valuable packages.

The wafer molding is conducted at ITRI. The mold dry film is 200 mm in diameter with 0.16 mm thickness, and the molding is conducted at 100 °C, with a post mold curing at 180 °C. Post molding inspection focused on delamination, mold surface quality, and wafer warpage, identifying some mold flashes around the edge, no delamination, and wafer warpage of less than 250 µm (see Fig. 9).

Figure 9. Molded resin wafer with Z-Coat 211 sacrificial layer on silicon carrier.

Figure 10. Wafer debonder Z-D200 from MMI.

E. Carrier Release with Air Jetting

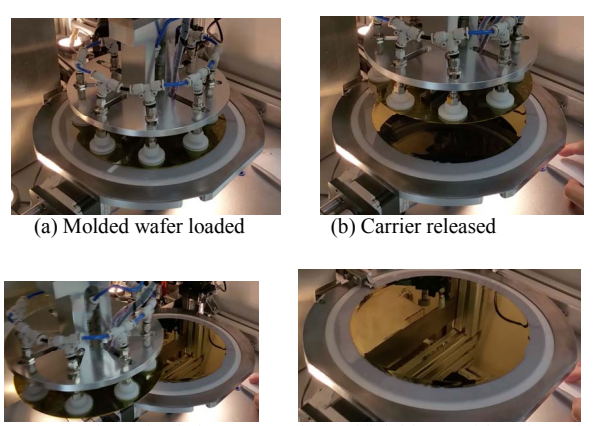
The carrier was released with air jetting by a semi-automatic wafer debonder (Z-D200, designed and manufactured by MMI) (Fig. 10). The debonder is equipped with an air jetting apparatus and is capable of releasing the carrier from the sacrifice layer within seconds. The patent-pending machine-vision and image-processing algorithm enables automated interface recognition to quickly identify the sacrifice layer, thus allowing precise air jetting to the interface between carrier and sacrifice layer at room temperature.

Fig. 11 shows images of the debonding sequence. Carrier release via air jetting proceeds as follows: (1) a dicing tape is laminated onto the molded wafer surface; (2) the molded wafer is transferred onto the debonding platform with the carrier on top and the tape on bottom; (3) vacuum is applied to the wafer vacuum station and suction cup; (4) the interface between the sacrifice layer and the carrier is detected; (5) the sacrifice layer is pierced from the edge of the carrier to create an air vent; (6) air is injected into the vent to push the carrier up, with suction cup lifting from the top, leaving the sacrifice layer with the molded wafer after separation; (7) the carrier is unloaded onto a cassette; (8) the vacuum is released and the molded wafer is removed from the station.

F. Removal of Sacrificial Layer with Cleaner

The sacrificial layer is designed on a carrier to undertake the build-up of FOWLP. After the FOWLP structure is built, the sacrificial layer must be completely removed prior to solder ball attachment. As the sacrifice layer is very thin and adheres to the passivation layer sufficiently well to withstand standard WLP processing, Z-Clean 830 is designed to wet etch the sacrifice layer away without damaging the passivation layer and molded wafer.

Fig. 12 shows the Z-Coat 211 partially removed from a piece of molded wafer by Z-Clean 830. A small area of Ti/Cu layer and molding compound were also exposed through polishing. Electrical testing on each layer (as in Fig. 13) was also conducted for verification purpose.



(a) Molded wafer loaded (b) Carrier released

(c) Carrier unloaded (d) Sacrificial layer with resin wafer

Figure 11. Images of the carrier release sequence.

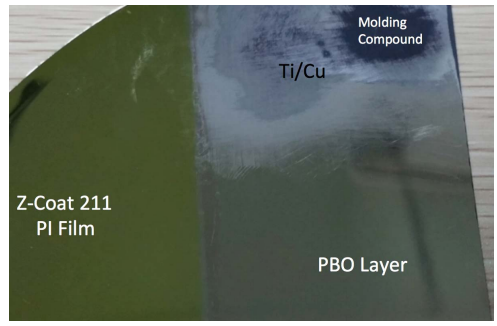


Figure 12. A piece of molded wafer exposes different layers

Figure 13. Electrical testing to identify each layer

V. SUMMARY

Carrier release with air jetting was carefully demonstrated for RDL-first fan out wafer level packaging. A polyimide-based spin-on solution Z-coat 211 is developed as the sacrificial layer after being baked to dry film. Z-Coat 211 has very low peel adhesion on silicon and glass but high thermostability and excellent chemical resistivity. With Z-Coat 211 as the sacrifice layer, the carrier can be detached from the molded reconstituted resin wafer with air jetting. The current sacrifice layer material also demonstrates sufficient shear strength and thermostability to support all fan-out wafer-level processes. After the carrier is released, liquid cleaner Z-Clean 830 completely removes the sacrificial layer through spray and rinse. The passivation layer, metal layer, and molded surface all are kept intact with no sign of any damage. Electrical conductivity testing on and between each layer was performed to ensure correct identification of each layer.

ACKNOWLEDGMENT

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REFERENCES

[1] C.F. Tseng, C.S. Liu, C.H. Wu and Douglas Yu N. Sn, "Info (Wafer Level Integrated Fan-Out) Technology" 2016 IEEE 66th Electonics Components and Technology Conference (ECTC), 2016. Las Vegas, NV, pp.1-6, May 31~June 3 2016.

[2] M. Brunnbauer, E. Furgut, G. Beer and T. Meyer, "Embedded wafer level ball grid array (eWLB)" Proc 8th Electonics Packaging Technology Conference (EPTC), 2006. pp.1-5, Dec 2016.

[3] C.C. Liu, C.S. Liu, C.H. Wu and Douglas Yu N. Sn, "High performance integrated fan-out wafer level packaging (InFO-WLP): Technology and System integration" Proc. IEEE Int. Electron Devices Meeting, Info (Wafer Level Integrated Fan-Out) Technology" pp.323-326, Dec 2012.

[4] D. Yu, "A new integration technology platform: integrated fan-out wafer-level-packaging for mobile applications," Symp. On VLSI Technology., pp.T46- T47, June 2015.

[5] H. Tang, C. Luo, M. Yin, Y.S Zeng and W.Zhang, "High throughput air jetting wafer debonding for 3D IC and MEMS manufacturing" 2016 IEEE 66th Electonics Components and Technology Conference (ECTC), 2016. Las Vegas, NV, pp.1678-1684, May 31~June 3 2016.